What is claimed is:

- 1 1. A semiconducting device comprising:
- 2 a substrate;
- a first die attached to the substrate, the first die including active circuitry on
- 4 an upper surface;
- a spacer covering the active circuitry on the upper surface of the first die, the
- 6 spacer extending from a first side of the first die to an opposing second side of the
- 7 first die and extending near a third side of the first die and an opposing fourth side
- 8 of the first die such that the active circuitry is exposed near the third and fourth sides
- 9 of the first die; and
- a second die stacked onto the spacer and the first die.
- 1 2. The semiconducting device of claim 1, wherein the active circuitry on the
- 2 upper surface of the first die includes a flash memory array.
- 1 3. The semiconducting device of claim 1, wherein the spacer is attached to the
- 2 upper surface of the first die using an adhesive.
- 1 4. The semiconducting device of claim 1, wherein the spacer includes at least
- 2 one section that extends to the third side of the first die such that the active circuitry
- 3 is only partially exposed near the third side of the first die.
- 1 5. The semiconducting device of claim 4, wherein the spacer includes at least
- 2 one section that extends to the fourth side of the first die such that the active
- 3 circuitry is only partially exposed near the fourth side of the first die.
- 1 6. The semiconducting device of claim 1, wherein the spacer is about 1mm
- 2 away from the third and fourth sides of the first die.

- 1 7. The semiconducting device of claim 1, wherein the spacer is formed of
- 2 silicon.
- 1 8. The semiconducting device of claim 1, further comprising at least one
- 2 additional die stacked onto the first die, the spacer and the second die.
- 1 9. The semiconducting device of claim 1, further comprising at least one
- 2 additional die mounted on the substrate, the first die being stacked onto the at least
- 3 one additional die.
- 1 10. The semiconducting device of claim 1, wherein the second die is attached to
- 2 the spacer using an adhesive.
- 1 11. The semiconducting device of claim 1, further comprising wires bonded to
- 2 pads that are part of the exposed active circuitry near the third and fourth sides of
- 3 the first die.
- 1 12. A method comprising:
- 2 securing a first die to a substrate, the first die including active circuitry on an
- 3 upper surface;
- 4 covering the active circuitry on the upper surface of the first die with a
- 5 spacer that extends from a first side of the first die to an opposing second side of the
- 6 first die, the spacer extending near a third side of the first die and an opposing fourth
- 7 side of the first die such that the active circuitry is exposed near the third and fourth
- 8 sides of the first die; and
- 9 stacking a second die onto the spacer and the first die.
- 1 13. The method of claim 12, wherein stacking the second die onto the spacer and
- 2 the first die includes securing the second die to the spacer with an adhesive.

- 1 14. The method of claim 12, further comprising stacking at least one additional
- 2 die onto the second die.
- 1 15. The method of claim 12, further comprising securing at least one additional
- 2 die between the first die and the substrate.
- 1 16. The method of claim 12, wherein covering the active circuitry on the first die
- 2 with a spacer includes covering the active circuitry where at least one section of the
- 3 spacer extends to the third side of the first die such that only a portion of the active
- 4 circuitry is exposed near the third side of the first die.
- 1 17. The method of claim 16, wherein covering the active circuitry on the first die
- 2 with a spacer includes covering the active circuitry where at least one section of the
- 3 spacer extends to the fourth side of the first die such that only a portion of the active
- 4 circuitry is exposed near the fourth side of the first die.
- 1 18. The method of claim 12, wherein covering the active circuitry such that the
- 2 spacer extends near a third side of the first die and a fourth side of the first die
- 3 includes covering the active circuitry such that the spacer is about 1mm away from
- 4 the third and fourth sides of the first die.
- 1 19. The method of claim 12, wherein covering the active circuitry on the first die
- with a spacer includes attaching the spacer to the active circuitry with an adhesive.
- 1 20. The method of claim 12, wherein covering the active circuitry on the first die
- with a spacer includes covering a portion of a flash memory array on the first die
- 3 with the spacer.
- 1 21. The method of claim 12, further comprising bonding wires to pads that are
- 2 part of the exposed active circuitry near the third and fourth sides of the first die.

- 22. An electronic system comprising:
- 1 a buss;
- a memory coupled to the buss; and
- a semiconducting device that is electrically connected to the buss, the
- 4 semiconducting device including a substrate and a flash memory that is attached to
- 5 the substrate, the flash memory including active circuitry on an upper surface, the
- 6 semiconducting device further including a spacer covering the active circuitry on
- 7 the upper surface of the flash memory and a die that is stacked onto the spacer and
- 8 the flash memory, the spacer extending from a first side of the flash memory to an
- 9 opposing second side of the flash memory and extending near a third side of the
- 10 flash memory and an opposing fourth side of the flash memory such that the active
- circuitry is exposed near the third and fourth sides of the flash memory.
- 1 23. The electronic system of claim 22, wherein the spacer includes at least one
- 2 section that extends to the third side of the flash memory such that the active
- 3 circuitry is only partially exposed near the third side of the flash memory.
- 1 24. The electronic system of claim 23, wherein the spacer includes at least one
- 2 section that extends to the fourth side of the flash memory such that the active
- 3 circuitry is only partially exposed near the fourth side of the flash memory.
- 1 25. The electronic system of claim 22, further comprising a voltage source
- 2 electrically coupled to the semiconducting device.
- 1 26. The electronic system of claim 22, further comprising wires bonded to pads
- 2 that are part of the exposed active circuitry near the third and fourth sides of the
- 3 flash memory, the wires being electrically coupled to the substrate.